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DATA SHEET

TDA1387T
Stereo Continuous Calibration DAC (CC-DAC)

Preliminary specification
Supersedes data of September 1994
File under Integrated Circuits, IC01

1995 Dec 11

Philips Semiconductors

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Stereo Continuous Calibration DAC (CC-DAC) TDA1387T

FEATURES

- Low power consumption
- Low total harmonic distortion
- Wide dynamic range (16-bit resolution)
- Continuous Calibration (CC) concept
- Single 3 to 5.5 V supply rail
- Output and bias current are proportional to the supply voltage
- Fast settling time enables 2, 4 and 8 times oversampling (serial input) or double-speed operation at 4 times oversampling
- Internal bias current ensures maximum dynamic range
- Wide operating temperature range (–40 to + 85 °C)
- I^2S-bus input format (time multiplex, two's complement, TTL)
- No zero-crossing distortion
- Large DC output voltage compliance
- Contained in small outline package.

APPLICATIONS

- Portable digital audio equipment.

GENERAL DESCRIPTION

The TDA1387T is a member of a generation of digital-to-analog converters which incorporates the innovative technique of Continuous Calibration. The largest bit currents are repeatedly generated from one single reference current. This duplication is based upon an internal charge storage principle and has an accuracy which is insensitive to ageing, temperature and process variations.

The TDA1387T is fabricated in a 1.0 μm CMOS process and features an extremely low power dissipation, small package size and easy application. The intrinsic high coarse current accuracy combined with the implemented symmetrical offset decoding method preclude zero-crossing distortion and ensure high quality audio reproduction. The CC-DAC is eminently suitable for use in portable digital audio equipment.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1387T	SO8	plastic small outline package; 8 leads; body width 3.9 mm.	SOT96-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		3.0	5.0	5.5	V
I_{DD}	supply current	V_{DD} = 5 V at code 0000H	–	5.5	6.5	mA
I_{FS}	full scale output current	V_{DD} = 5 V	0.86	1.0	1.14	mA
		V_{DD} = 3 V	–	0.6	–	mA
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB signal level	–	–88	–78	dB
		at 0 dB signal level	–	0.004	0.012	%
		at –60 dB signal level	–	–33	–24	dB
		at –60 dB signal level	–	2.2	6	%
		at –60 dB; A-weighted	–	–35	–	dB
		at –60 dB; A-weighted	–	1.7	–	%
S/N	signal-to-noise ratio at bipolar zero	A-weighted at code 0000H	86	98	–	dB
t_{cs}	current settling time to ±1 LSB		–	0.2	–	µs
BR	input bit rate (pin 3)		–	–	18.4	Mbits/s
f_{clk}	clock frequency		–	–	18.4	MHz
TC_{FS}	full scale temperature coefficient at pins 6 and 8		–	$\pm 400 \times 10^{-6}$	–	
T_{amb}	operating ambient temperature		–40	–	+85	°C
P_{tot}	total power dissipation	V_{DD} = 5 V at code 0000H	–	27.5	36	mW
		V_{DD} = 3 V at code 0000H	–	10	–	mW

BLOCK DIAGRAM

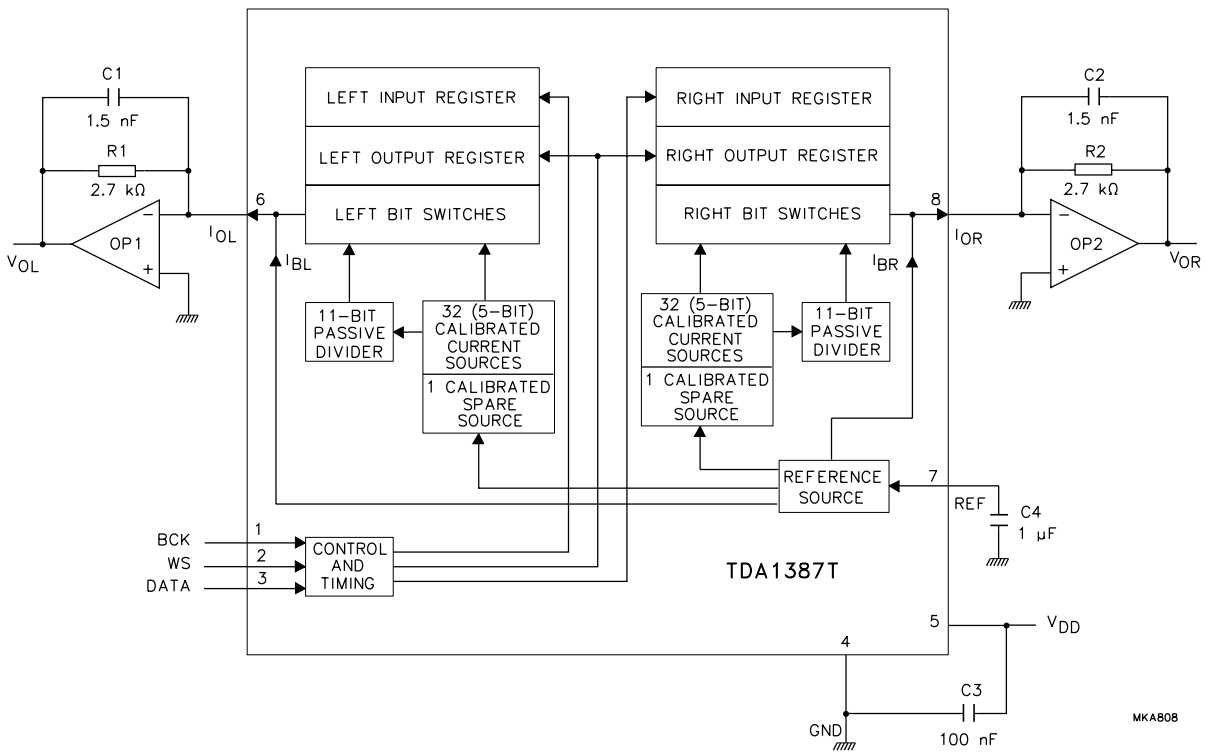


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
BCK	1	bit clock input
WS	2	word selection input
DATA	3	data input
GND	4	ground
V_{DD}	5	supply voltage input
I_{OL}	6	left channel output
REF	7	reference decoupling
I_{OR}	8	right channel output

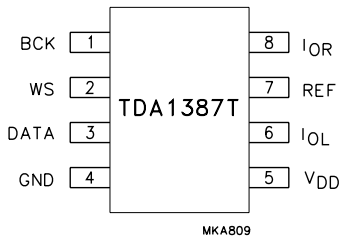


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The basic operation of the continuous calibration DAC is illustrated in Fig.3 which shows the calibration and operation cycle. During calibration of the MOS current source (Fig.3a) transistor M1 is connected as a diode by applying a reference current. The voltage V_{gs} on the intrinsic gate-source capacitance C_{gs} of M1 is then determined by the transistor characteristics. After the drain current has been calibrated to the reference value I_{ref}, the switch S1 is opened and S2 is switched to the other position (Fig.3b). The gate-to-source voltage V_{gs} of M1 is not changed because the charge on C_{gs} is preserved. Therefore, the drain current of M1 will still be equal to I_{ref} and this exact duplication of I_{ref} is now available at the OUT terminal.

In the TDA1387T, 32 current sources and one spare current source are continuously calibrated (see Fig.1). The spare current source is included to allow continuous converter operation. The output of one calibrated source is connected to an 11-bit binary current divider which consists of 2048 transistors. A symmetrical offset decoding principle is incorporated and arranges the bit switching such that the zero-crossing is performed by switching only the LSB currents.

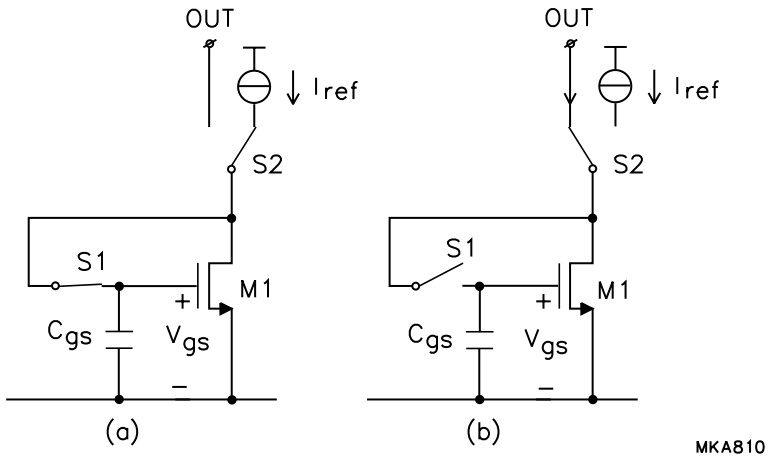
The TDA1387T (CC-DAC) accepts serial input data format of 16-bit word length. Left and right data words are time multiplexed. The input data format is shown in Figs 4 and 5.

With a HIGH level on the WS input, data is placed in the right input register, with a LOW level on the WS input, data is placed in the left input register. The data in the input registers are simultaneously latched to the output registers which control the bit switches. An internal bias current I_{bias} is added to the full scale output current I_{FS} in order to achieve maximum dynamic range at the outputs of OP1 and OP2.

The signal current I_{FS} and the bias current I_{bias} are both proportional to the supply voltage V_{DD}, and have a fixed mutual relation A_{bias} (where $A_{bias} = I_{bias}/I_{FS}$).

It is preferred that the non-inverting input of operational amplifiers OP1 and OP2 is tied to ground to achieve a maximum dynamic range over the supply voltage range.

A decoupling capacitor C4 is recommended for enhancing the supply voltage ripple rejection of the DAC. It has no significant effect on the noise performance.



(a) Calibration.
(b) Operation.

Fig.3 Calibration principle.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	DESCRIPTION	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		–	6.0	V
$T_{xtal(max)}$	maximum crystal temperature		–	+150	°C
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		–40	+85	°C
V_{es}	electrostatic handling	note 1	–2000	+2000	V
		note 2	–200	+200	V

Notes

1. Human body model: C = 100 pF; R = 1.5 kΩ; 3 zaps positive and 3 zaps negative.
2. Machine model: C = 200 pF; L = 0.5 μH; R = 10 Ω; 3 zaps positive and 3 zaps negative.

THERMAL CHARACTERISTICS

SYMBOL	DESCRIPTION	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	210	K/W

CHARACTERISTICS

V_{DD} = 5 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		3.0	5.0	5.5	V
I_{DD}	supply current	at code 0000H	–	5.5	6.5	mA
SVRR	supply voltage ripple rejection	note 1	–	30	–	dB
Digital inputs; WS, BCK and DATA						
$\|I_{LI}\|$	LOW level input leakage current	V_i = 0 V	–	–	10	µA
$\|I_{HI}\|$	HIGH level input leakage current	V_i = 5 V	–	–	10	µA
f_{BCK}	clock frequency		–	–	18.4	MHz
BR	data bit rate		–	–	18.4	Mbits/s
f_{WS}	word select input frequency		–	–	384	kHz
Timing						
t_r	rise time		–	–	12	ns
t_f	fall time		–	–	12	ns
T_{cy}	bit clock cycle time		54	–	–	ns
t_{HB}	bit clock HIGH time		15	–	–	ns
t_{LB}	bit clock LOW time		15	–	–	ns
$t_{su;DA}$	data set-up time		12	–	–	ns
$t_{h;DA}$	data hold time		2	–	–	ns
$t_{h;WS}$	word select hold time		2	–	–	ns
$t_{su;WS}$	word select set-up time		12	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog outputs; I_{OL} and I_{OR}						
RES	output resolution		–	–	16	bits
V_{DCC}	DC output voltage compliance		0	–	3.5	V
$I_{o(p-p)}$	AC output signal current (peak-to-peak value)	note 2	0.86	1.0	1.14	mA
TC_{FS}	full-scale temperature coefficient		–	$\pm 400 \times 10^{-6}$	–	
I_{bias}	output bias current	note 2	0.93	1.08	1.23	mA
V_{ref}	output reference voltage	note 2	–	$\frac{1}{6}V_{DD}$	–	V
R_{ref}	output resistance at pin 7		7.6	11.4	14.8	kΩ
(TDH + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB signal level; note 3	–	–88	–78	dB
		at 0 dB signal level; note 3	–	0.004	0.01	%
		at –60 dB signal level; note 3	–	–33	–24	dB
		at –60 dB signal level; note 3	–	2.2	6	%
		at –60 dB; A-weighted; note 3	–	–35	–	dB
		at –60 dB; A-weighted; note 3	–	1.8	–	%
		f_i = 20 Hz to 20 kHz; at 0 dB signal level; note 3	–	–84	–70	dB
		f_i = 20 Hz to 20 kHz; at 0 dB signal level; note 3	–	0.006	0.03	%
t_{cs}	current settling time to ±1 LSB		–	0.2	–	µs
α_{cs}	channel separation		86	95	–	dB
$\lvert\Delta I_O\rvert$	unbalance between outputs	note 3	–	0.2	0.3	dB
$\lvert t_d\rvert$	delay time between outputs		–	±0.2	–	µs
S/N	signal-to-noise ratio at bipolar zero	A-weighted at code 0000H	86	98	–	dB

Notes

1. V_{ripple} = 1% of the supply voltage; f_{ripple} = 100 Hz.
2. Values are proportional to V_{DD}.
3. Measured with 1 kHz sine wave generated at a sampling rate of 192 kHz.

QUALITY SPECIFICATION

In accordance with *"SNW-FQ-611E"*. The numbers of the quality specification can be found in the *"Quality Reference Handbook"*. The handbook can be ordered using the code 9397 750 00192.

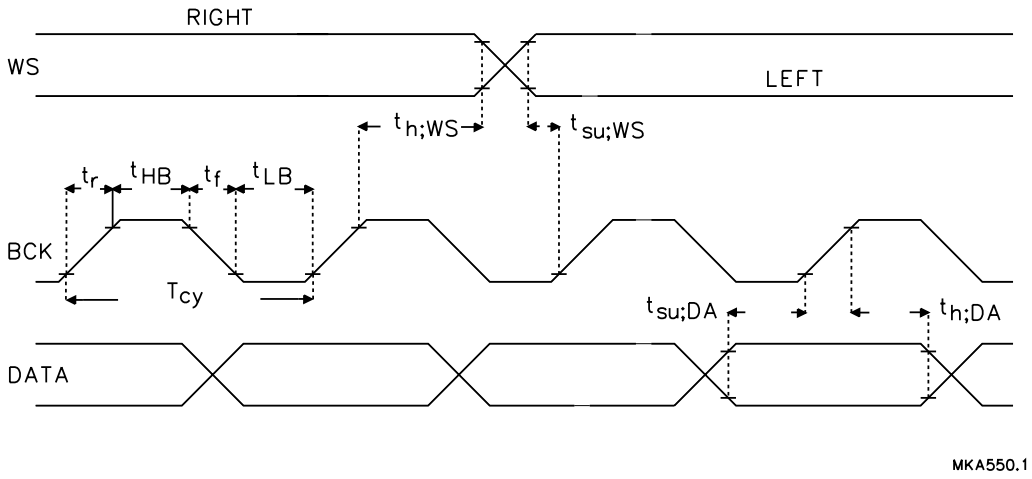


Fig.4 Input signal timing (I^2S-bus).

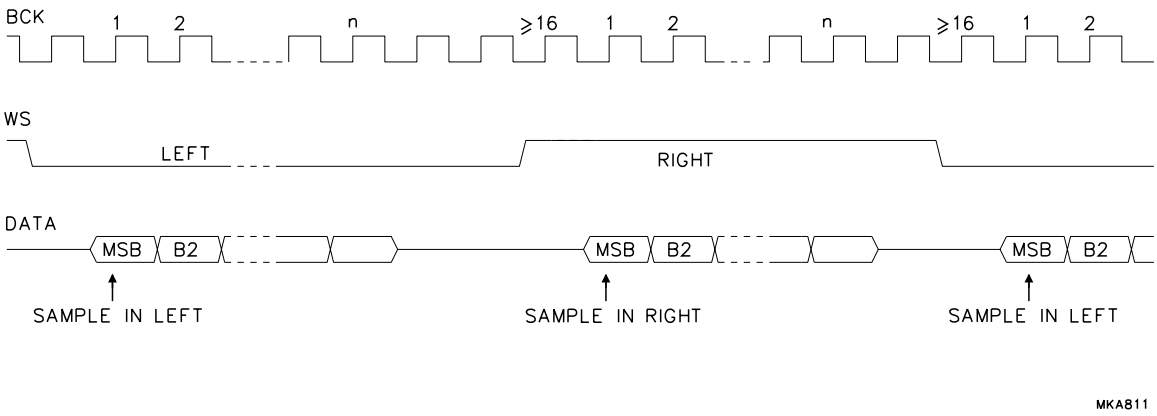


Fig.5 Input signal format (I^2S-bus).

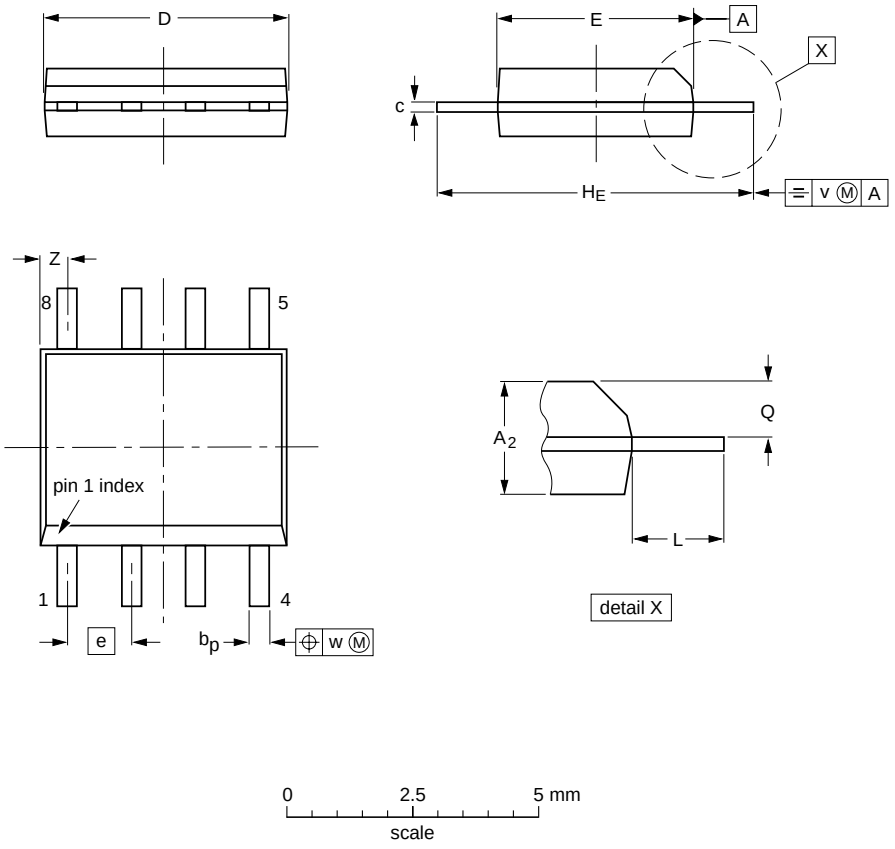
APPLICATION INFORMATION

The TDA1387T offers great ease in designing-in to printed-circuit board due to its small size and low pin count. The TDA1387T being a mixed-signal IC in CMOS, some attention needs to be paid to layout and topology of the application PCB. The following basic rules will yield the desired performance. The most important considerations are:

1. Supply: care should be taken to supply the TDA1387T with a clean, noiseless supply voltage, for a good noise performance of the analog parts of the DAC. Supply purity can easily be achieved by using an RC-filtered supply.
2. Grounding: preferably a ground plane should be used, in order to have a low-impedance return available at any point in the layout. It is advantageous to make a partitioning of the ground plane according to the nature of the expected return currents (digital input returns separate from supply returns separate from the analog section).
3. Topology: the capacitor decoupling high-frequency supply interference from V_{DD} to GND should be placed as close as is physically possible to the IC body, ensuring a low-inductance path to ground. The digital input conductors may be shielded by ground leads running alongside. The placement of a passive ground plane underside the entire IC surface gives ‘free’ additional decoupling from the IC body to ground as well as providing a shield between the digital input pins and the analog output pins.

PACKAGE OUTLINE

SO8: plastic small outline package; 8 leads (straight); body width 3.9 mm **SOT96-2**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A_2	b_p	c	D(1)	E(2)	e	H_E	L	Q	v	w	Z(1)
mm	1.45 1.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.4 6.2	1.2	0.7 0.6	0.25	0.25	0.7 0.3
inches	0.057 0.049	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.252 0.244	0.047	0.028 0.024	0.01	0.01	0.028 0.012

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-2						~~95-02-04~~ 97-05-22

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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NOTES

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